IN THE ~~UNITED STATES PATENT AND~~ TRADEMARK OFFICE

Applicant: Kiran Ganesh et al.
Serial No.: 09/431,477
Filed: November 1, 1999
Title: 2-DIMENSIONAL PLACEMENT WITH RELIABILITY CONSTRAINTS FOR VLSI DESIGN

Examiner: Phallaka Kik
Group Art Unit: 2825
Docket: 884.141US1

Amdt 7/A 4/16/02 Allowed

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on September 25, 2001. Please amend the above-identified patent application as follows.

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a three-month extension of the period for responding to the Office action, thereby moving the deadline for response from December 25, 2001, to March 25, 2001.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claims 3, 9, 24 and 28; and amendment of previously pending claims 1, 2, 7, 8, 22, 26, 29 and 31. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. [Amended] A computerized method of creating a layout for a circuit design, the method comprising:

receiving a circuit design;

receiving at least one layout rule based on a reliability verification constraint arising from self heat [for the circuit design]; and

generating a layout for the circuit design through computer automated operations wherein the layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.